

What is claimed is:

Claims:

- 1 1. A semiconductor structure comprising:
2 an active layer of a semiconductor material, said active layer including a strained
3 region;
4 a substrate; and
5 an insulating layer disposed between said active layer and said substrate, said
6 insulating layer containing a thickened region underlying said strained region, and said
7 thickened region transferring tensile stress to said strained region.
- 1 2. The semiconductor structure of claim 1 wherein said insulating layer is a buried
2 oxide layer and said active layer is silicon.
- 1 3. The semiconductor structure of claim 1 further comprising:
2 a source defined in said active layer;
3 a drain defined in said active layer; and
4 a channel defined in a portion of said active layer between said source and said
5 drain, said channel disposed at least partially in said strained region of said active layer.
- 1 4. The semiconductor structure of claim 3 further comprising:
2 a gate electrode electrically isolated from said portion of said active layer defining
3 said channel.
- 1 5. The semiconductor structure of claim 4 wherein said strained region divides said
2 gate electrode.

1 6. The semiconductor structure of claim 4 wherein said gate electrode generally
2 overlies said channel.

1 7. The semiconductor structure of claim 1 further comprising:
2 a semiconductor device fabricated using said active layer.

1 8. The semiconductor structure of claim 1 wherein said active layer is silicon and said
2 thickened region of said insulating layer is formed by oxidation of said active layer.

1 9. The semiconductor structure of claim 9 wherein said insulating layer is silicon
2 dioxide.

1 10. The semiconductor structure of claim 9 wherein said substrate is silicon and said
2 thickened region is formed by oxidation of said substrate.

1 11. The semiconductor structure of claim 1 wherein said tensile stress is effective to
2 enhance carrier mobility within said strained region.

1 12. The semiconductor structure of claim 1 wherein a thickness of said thickened region
2 is increased by an increment in the range of about 5 nanometers to about 10 nanometers.

1 13. The semiconductor structure of claim 1 wherein said thickened region of said
2 insulating layer has a thickness greater than that of surrounding regions of said insulating
3 layer flanking said thickened region.

1 14. The semiconductor structure of claim 1 further comprising:
2 first and second anchors flanking said strained region, said first and second anchors
3 effective for limiting relaxation of said strained region of said active layer.

- 1 15. The semiconductor structure of claim 16 wherein said first and second anchors
- 2 comprise adjacent regions of said active layer flanking said strained region.

1 16. A method of fabricating a strained semiconductor structure, comprising:
2 selectively oxidizing an active layer locally at a location between the active layer
3 and an underlying insulating layer so as to increase a thickness of the insulating layer across
4 a thickened region, the thickened region inducing tensile stress in the active layer to thereby
5 form a strained region in the active layer overlying the thickened region.

1 17. The method of claim 16 wherein the active layer is silicon, and selectively oxidizing
2 the insulating layer comprises:
3 reacting the active layer with a gaseous oxidizing species diffusing in the insulating
4 layer from an ambient environment to form the thickened region of the insulating layer.

1 18. The method of claim 17 wherein selectively oxidizing the insulating layer
2 comprises:
3 covering the insulating layer and the active layer with an oxidation mask; and
4 forming windows in the oxidation mask that permit transport of a gaseous oxidizing
5 species into the insulating layer for subsequent diffusion to the thickened region.

1 19. The method of claim 18 wherein covering the insulating layer and the active layer
2 comprises:
3 forming a patterned layer of silicon nitride.

1 20. The method of claim 16 further comprising:
2 forming a source and a drain in the active layer, the source and the drain flanking a
3 channel defined at least partially in the strained region of the active layer.

- 1 21. The method of claim 20 further comprising:
2 forming a gate electrode electrically isolated from the active layer and overlying the
3 channel.
- 1 22. The method of claim 21 wherein the strained region divides the gate electrode.
- 1 23. The method of claim 16 further comprising:
2 selectively oxidizing a portion of a substrate supporting the insulating layer at a
3 location underlying the strained region so as to increase the thickness of the overlying
4 insulating layer in the thickened region.
- 1 24. The method of claim 23 wherein the insulating layer comprises silicon dioxide and
2 the substrate comprises silicon.
- 1 25. The method of claim 16 wherein the insulating layer comprises silicon dioxide and
2 the active layer comprises silicon.

- 1 26. A method of fabricating a strained semiconductor structure, comprising:
2 thickening a thickened region of an insulating layer at a location underlying a
3 strained region of an active layer so as to induce tensile stress in the active layer and thereby
4 form the strained region in the active layer.
- 1 27. The method of claim 26 wherein thickening the thickened region further comprises:
2 selectively oxidizing the active layer at an interface between the active layer and the
3 insulating layer so as to locally increase a thickness of the thickened region.
- 1 28. The method of claim 27 wherein the active layer is silicon, and thickening the
2 thickened region comprises:
3 reacting the active layer with a gaseous oxidizing species diffusing in the insulating
4 layer from an ambient environment to a location beneath the strained region for forming the
5 thickened region of the insulating layer.
- 1 29. The method of claim 28 wherein reacting the active layer comprises:
2 covering the insulating layer and the active layer with an oxidation mask; and
3 forming windows in the oxidation mask that permit transport of a gaseous oxidizing
4 species into the insulating layer for subsequent diffusion.
- 1 30. The method of claim 29 wherein covering the insulating layer and the active layer
2 comprises:
3 forming a patterned layer of silicon nitride.
- 1 31. The method of claim 26 further comprising:
2 forming a source and a drain in the active layer, the source and the drain flanking a
3 channel defined at least partially in the strained region of the active layer.

1 32. The method of claim 31 further comprising:
2 forming a gate electrode electrically isolated from the active layer and overlying the
3 channel.

1 33. The method of claim 32 wherein the strained region divides the gate electrode.

1 34. The method of claim 26 further comprising:
2 selectively oxidizing a substrate supporting the insulating layer at a location
3 underlying the strained region so as to increase the thickness of the overlying insulating
4 layer in the thickened region.